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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,886	02/11/2002	Gregory S. Snider	10008139-1	3539

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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
AMIN, NIRAV S	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,886	SNIDER, GREGORY S.	
	Examiner	Art Unit	
	Nirav S. Amin	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-26 are presented in the application.

The rejection is respectfully maintained and reproduced infra for applicant's convenience.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bowen (Appl. S/N: 09/771,963) in view of Garey (USPN: 6,662,302).

As per claim 1, Bowen teaches:

parsing a source code [Para. [0113]];

performing a plurality of optimizations on the parsed code [Para. [0113]];

generating a configuration instruction set based on the optimized source code [Para. [0298], Figure 11];

Bowen does not teach automatically selecting one of the generated configuration instruction sets according to a user-defined criteria.

Garey teaches:

automatically selecting one of the plurality of generated configuration instruction sets according to a user-defined criteria, the selected configuration instruction set being

used to configure hardware [Column 3, lines 32-45; The alternative logic configuration is chosen in response to the input data, the input data is viewed as the user criteria.]

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Bowen and Garey to obtain a circuit which can perform a wide variety of operations to accommodate various pluralities of input data [Column 1, lines 40-42].

As per claim 11, Bowen teaches:

generating an internal representation of the source code [(1104), Figure 11];

analyzing data flow properties of the internal representation in order to optimize the internal representation [Para. [0113]];

automatically generating a configuration instruction set based on the optimized internal representation [(1106), Figure 11];

generating a plurality of configuration instruction sets based on the optimized source code [(1106), Figure 11]; and

Bowen does not expressly teach automatically selecting one of the generated configuration instruction sets according to a user-defined criteria.

Garey teaches:

automatically selecting one of the plurality of generated configuration instruction sets according to a user defined criteria, the selected configuration instruction set being used to configure hardware [Column 3, lines 32-45; The alternative logic configuration is chosen in response to the input data, the input data is viewed as the user criteria.].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Bowen and Garey to obtain a circuit which can perform a wide variety of operations to accommodate various pluralities of input data [Column 1, lines 40-42].

As per claim 17, Bowen teaches:

a processor (1010) operable to receive source code;

a complier (302, Figure 3) automatically generating a configuration set from the received source code; and

a configurable hardware device receiving the selected configuration instruction set and being configured based on the received configuration instruction set (1108, Figure 11).

Bowen does not expressly teach selecting one of the plurality of configuration sets based on user defined criteria.

Garey teaches:

selecting one of the plurality of generated configuration instruction sets according to a user defined criteria [Column 3, lines 32-45; The alternative logic configuration is chosen in response to the input data, the input data is viewed as the user criteria.].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Bowen and Garey to obtain a circuit which can perform a wide variety of operations to accommodate various pluralities of input data [Column 1, lines 40-42].

As per claim 23, Bowen teaches:

means for parsing a source code (204, Figure 2);

means for performing a plurality of optimizations on the parsed code [Para. [0113]];

means for generating a configuration instruction set based on the optimized source code (1106, Figure 11);

Bowen does not expressly teach:

means for automatically selecting one of the plurality of generated configuration instruction sets according to a user-defined criteria.

Garey teaches:

automatically selecting one of the plurality of generated configuration instruction sets according to a user-defined criteria, the selected configuration instruction set being used to configure hardware [Column 3, lines 32-45; The alternative logic configuration is chosen in response to the input data, the input data is viewed as the user criteria.].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Bowen and Garey to obtain a circuit which can perform a wide variety of operations to accommodate various pluralities of input data [Column 1, lines 40-42].

As per claims 3, 14 and 25, Garey teaches:

determining characteristics for the each of the plurality of the configurable instruction sets and selecting one of the plurality of configuration instructions sets based

on determined the characteristics of that set, wherein the characteristics are associated with the user-defined criteria [Column 3, lines 39-49].

As per claims 4 and 26, Garey does not expressly teach receiving simulation results associated with each configuration instruction set. At the time of the invention it would be obvious to a person of ordinary skill in the art to receive simulation results of each configuration instruction set.

As per claims 7 and 15, Bowen teaches:

the user defined criteria is the speed to complete a computation, size of circuit [Para. [0123]. Bowen does not expressly teach the user defined criteria is circuit power. Garey teaches the user defined criteria is circuit power [Column 3, lines 45-49]. At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the teachings of Bowen and Garey to include more test parameters.

As per claims 8 and 19, Bowen teaches generating an internal representation of the source code [(1104), Figure 11];

As per claims 9 and 16, Bowen teaches configuring hardware using the selected configuration instruction set [(1108), Figure 11].

As per claim 10, Bowen teaches using the selected configuration instruction set to configure an FPGA or a custom integrated circuit [Para. 0298].

Response to Arguments

Applicant's arguments filed 03/15/2005 have been fully considered but they are not persuasive.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Furthermore, the test of obviousness is:

> "whether the teachings of the prior art, taken as a whole, would have made obvious the claimed invention," *In re Gorman*, 933 F.2d at 986, 18 USPQ2d at 1888.
>
> Subject matter is unpatentable under section 103 if it "'would have been obvious . . . to a person having ordinary skill in the art.' While there must be some teaching, reason, suggestion, or motivation to combine existing elements to produce the claimed device, it is not necessary that the cited references or prior art specifically suggest making the combination." *In re Nilssen*, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988).

"Such suggestion or motivation to combine prior art teachings can derive solely from the existence of a teaching, which one of ordinary skill in the art would be presumed to know, and the use of that teaching to solve the same [or] similar problem which it addresses." *In re Wood*, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (CCPA 1979).

"In sum, it is off the mark for litigants to argue, as many do, that an invention cannot be held to have been obvious unless a suggestion to combine prior art teachings is found *in* a specific reference."

Entire quote from *In re Oetiker*, 24 USPQ2d 1443 (CAFC 1992).

To further explain the Bowen - Garey combination, Bowen teaches a process for compiling a C function to a reconfigurable logic device. A function written in a C programming language is received, parsed and optimized. The C function is compiled into processor instructions in operation 1104. In operation 1106, the processor instructions are used to generate hardware configuration information. In operation 1108, a Field Programmable Gate Array (FPGA) is configured using the hardware configuration information such that the function is compiled to the FPGA. Bowen also discloses that the methodology of the invention could also be applied to compile functions to reconfigurable logic devices other than FPGAs.

Garey teaches in figure 4, a logic configuration selection circuitry that selects at least one configuration option to program a programmable logic circuitry using various parameters including, among other things, a plurality of input data that is given to the processor.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nirav S. Amin whose telephone number is (571) 272-3821. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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